

UTILITY PATENT APPLICATION TRANSMITTAL UNDER 37 C.F.R. §1.53(b)

ASSISTANT COMMISSIONER FOR PATENTS

Box PATENT APPLICATION

Washington D.C. 20231

Case Docket No.: HI-004

Sir:

Submitted herewith for filing is the patent application of

INVENTOR OR APPLICATION IDENTIFIER: Wong Hyoung PARK

COURT NUMBER: A DEMODULATION APPARATUS OF A BASE STATION IN A CDMA MOBILE COMMUNICATION

SYSTEM

Enclosed are:

- 20 pages of specification, claims, abstract
 2 sheets of FORMAL drawing.
3. 2 pages of newly executed Declaration & Power of Attorney (original).
4. Priority Claimed.
5. Small Entity Statement.
6. Information Disclosure Statement, Form PTO-1449 and reference.
10. Authorization under 37 C.F.R. §1.136(a)(3).
11. Other:

7. Assignment Papers for LG Information & Communications, Ltd.
 (cover sheet, assignment & assignment fee).
8. Certified copy of Korean Patent Appln. No. 27090/1999, filed July 6, 1999.
9. Two (2) return postcards.
 Stamp & Return with Courier.
 Prepaid Postcard-Stamped Filing Date & Returned with Unofficial Serial Number.

CLAIMS AS FILED					
For	No. Filed		No. Extra	Rate	Fee
Total Claims	21	- 20	1	X \$18.00	\$ 18.00
Indep. Claims	3	- 3	0	X \$78.00	
Multiple Dependent Claims (If applicable)					
X \$260.00					
BASIC FEE					
TOTAL FILING FEE					
\$690.00					
\$708.00					

- [] This is a Continuation-in-part (CIP) of prior application No: _____ filed _____. Incorporation By Reference-The entire disclosure of the prior application is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
- [] Amend the specification by inserting before the first line the sentence:
 --This application is a continuation-in-part of Application Serial No. _____ filed _____.
- A check in the amount of \$ 708.00 (Check # 8768) is attached.
- [] Please charge my Deposit Account No. 16-0607 in the amount of \$ ____. A duplicate copy of this sheet is enclosed.
- The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 16-0607. A duplicate copy is enclosed.
- Any additional filing fees required under 37 C.F.R. 1.16.
- The Commissioner is hereby authorized to charge payment of following fees during the pendency of this application or credit any overpayment to Deposit Account No. 16-0607. A duplicate copy of this sheet is enclosed.
- Any patent application processing fees under 37 C.F.R. 1.17.
- Any filing fees under 37 C.F.R. 1.16 for presentation of extra claims.

FLESCHNER & KIM, LLP

Daniel Y.J. Kim
 Registration No. 36,186
 Anthony H. Nourse
 Registration No. 46,121

Correspondence Address Below:

P.O. Box 221200
 Chantilly, VA 20153-1200
 (703) 502-9440

Date: May 26, 2000

DYK/AHN jd

JC625 U.S. PTO
 09/57/9511

05/26/00

APPLICATION FOR UNITED STATES LETTERS PATENT

INVENTORS: Wong Hyoung PARK

TITLE: A DEMODULATION APPARATUS OF A BASE STATION IN A
CDMA MOBILE COMMUNICATION SYSTEM

ATTORNEYS:
& FLESHNER & KIM, LLP
ADDRESS: P. O. Box 221200
Chantilly, VA 20153-1200

DOCKET NO.: HI-004

A DEMODULATION APPARATUS OF A BASE STATION IN A CDMA MOBILE COMMUNICATION SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to a base station in a Code Division Multiple Access (CDMA) mobile communication system, and more particularly, to a demodulation apparatus of a base station in CDMA mobile communication system.

2. Background of the Related Art

Quadrature Phase Shift Keying (QPSK) demodulation in a mobile communication system may be accomplished by converting a high frequency signal received via an antenna into an intermediate frequency signal by using a mixer, and dividing the intermediate signal into an In-Phase channel (I channel) and a Quadra-Phase channel (Q channel) before demodulating to a base-band frequency signal with a demodulator. The analog base-band frequency signal thus demodulated into I and Q channels using the QPSK demodulation is then adjusted to a specific amplitude using a Low-Pass filter and an amplifier. Next, the signal is converted into a base-band digital signal, which is a CDMA signal, using an analog-to-digital converter. Finally, the CDMA signal is transferred to a CDMA modem for demodulation.

Figure 1 shows a block diagram illustrating a related art base station receiver of a mobile communication system. Referring to Figure 1, a signal transmitted from a mobile station is received through the base station antenna and relayed to a low noise amplifier 103 via the channel-pass filter 102. The low noise amplifier 103 then amplifies and outputs the signal, and passes it through the band-pass filter 104 and the high frequency amplifier 105. Next, the signal is converted into an intermediate frequency CDMA signal in the high frequency mixer 106.

The intermediate frequency CDMA signal then passes through a Surface Acoustic Wave (SAW) filter 107 and the intermediate frequency amplifier 108 to remove unnecessary signal components. The resulting signal is transmitted to the QPSK demodulator 109 where it is demodulated. The QPSK demodulator 109 outputs an I channel signal and a Q channel signal.

The high frequencies of the analog I channel and Q channel signals as demodulated by the QPSK demodulator 109 are removed by the low-pass filter 110. The filtered signals are then amplified by the base-band amplifier 111 to a specific amplitude compatible with the analog-to-digital conversion, and subsequently transferred to the Analog-to-Digital converter 112.

The Analog-to-Digital converter 112 converts the transmitted signal into a base-band digital signal. The base-band CDMA signal (i.e., the I channel and the Q channel converted to digital signals) is relayed to a CDMA modem 113 for demodulation.

Thereafter, the demodulated CDMA signal is transferred to the central office 114, for example a switching station, as a Pulse Code Modulation (PCM) signal.

The QPSK demodulation method of the related art system, however, has various problems. For example, the signal is divided into the analog base-band frequency signal with an I channel and a Q channel by the QPSK demodulator 109, and the divided signal is converted to the digital signal using the Analog-to-Digital converter 112. As a result, numerous circuit devices are needed, making the circuit diagram more complex, more expensive, and less efficient.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a demodulation system that substantially obviates one or more of the problems caused by the disadvantages of the related art.

Another object of the present invention is to provide a demodulator that can perform Quadrature Phase Shift Keying (QPSK) modulation and Analog-to-Digital Conversion using only a Analog-to-Digital Converter.

Another object of the present invention is to provide an apparatus for base station demodulation of a CDMA mobile communication system that can directly perform the QPSK demodulation and Analog-to-Digital Conversion using only an Analog-to-Digital Converter of a QPSK receiver compatible with the mobile communication system.

Another object of the present invention is to provide a demodulation system for a base station in a mobile communication system which is power efficient and cost effective.

To achieve at least the above objects in whole or in part, there is provided an apparatus for the base station demodulation in a CDMA mobile communication system having an analog-to-digital converter device to convert an intermediate frequency signal into a digital signal and provide a quadrature component and an in-phase component of the digital signal, a plurality of filters to filter the components of the digital signal in the low pass band respectively, and a CDMA modem to demodulate the outputs of the plurality of filters.

To achieve the above objects in whole or in part, there is further provided a signal processing device having a digital sampling device to sample the transferred intermediate frequency signal, a signal arbiter to distinguish the amplitude of the intermediate frequency signal passed through the digital sampling device, and a quantization device to convert the distinguished intermediate frequency signal to a digital signal, a latch device to hold the converted digital signal for a specific period of time before transferring to a plurality of channels, and an output device to transfer the digital signal to each channel of a plurality of channels to a plurality of filters at the specific transfer periods.

To further achieve the above-described objects of the present invention in a whole or in parts, there is provided a signal processor that includes a digitizer, which receives

and analog signal and generates a digital signal, a channel separator, which receives the digital signal from the digitizer and separates the digital signal into at least 2 channels, each channel having a different phase, and a phase shift controller, which receives a clock signal and controls the phase shifting of the channel separator.

5 To further achieve the above-described objects of the present invention in a whole or in parts, there is provided a demodulator for a CDMA receiver that includes an input circuit to amplify a filtered CDMA formatted input signal, a first signal processor to generate an intermediate frequency CDMA signal based on the amplified input signal, a second signal processor to output first and second digital signals on first and second channels, respectively, based on the intermediated frequency CDMA signal, the second signal processor having an analog-to-digital converter to convert the intermediate frequency CDMA signal to an intermediate digital signal and a channel separator to generate the first and second digital signals based on the intermediate digital signal, and an output circuit to output a demodulated output signal based on the first and second 15 digital signals, the output circuit having first and second Finite Impulse Response (FIR) filters to receive and filter the first and second digital signals, respectively, wherein the first and second digital signals have different phases.

Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having

ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objects and advantages of the invention may be realized and attained as particularly pointed out in the appended claims.

5

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements wherein:

Figure 1 is a block diagram of a related art mobile communication system.

Figure 2 is a block diagram showing a CDMA mobile communication system with a base station demodulation apparatus in accordance with a preferred embodiment of the present invention.

Figure 3 is a block diagram showing the Analog-to-Digital converter of Figure 2.

Figure 4 is a block diagram showing the internal circuit of the output formatter of Figure 3.

15

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Figure 2 illustrates the base station demodulation apparatus for a CDMA mobile communication system according to a preferred embodiment of the present invention. Elements 201 through 208 are similar to the related art base station receiver of the mobile communication system of Figure 1. The system as shown in Figure 2, however, uses an

Analog-to-Digital converter 209 as a signal processing device to perform both QPSK demodulation and Analog-to-Digital conversion.

As illustrated in Figure 3, the Analog-to-Digital converter 209 of the signal-processing device preferably includes a digital sampler 301 to sample the intermediate frequency signal received from the intermediate frequency amplifier 208, and a zero-order holder 302, which serves as a signal arbiter for distinguishing the amplitude of the intermediate frequency signal sampled by the digital sampler 301. A quantizer 303 then converts the distinguished intermediate frequency signal to a digital signal.

First, second, and third latch devices 304, 305 and 306 delay the converted digital signal for a prescribed time period before transferring it to a plurality of channels, for example, an I channel and Q channel, by way of first and second formatters 307 and 308. The first and second formatters 307 and 308 in turn periodically transmit the channel divided digital signals to a corresponding plurality of filters 210. The filters are preferably low pass filters, for example, a Finite Impulse Response (FIR) low pass filter. The system further includes a plurality of buffers 310 for buffering the transferred signal, and a D flip-flop 311.

Referring to Figure 4, the first and second formatters 307 and 308 are preferably provided with a plurality of negators 401 for negating the transferred signal and outputting the signal, and a plurality of selectors 402 of selecting one of the output signals of the negator 401 and the signal that has not passed through the negator 401.

The demodulation process of the base station signal will now be described.

Referring to Figures 2 and 3, the CDMA analog signal transferred to the Analog-to-Digital converter 209 from the intermediate frequency amplifier 208 is sampled by the digital sampler 301. At this time, the prescribed sampling frequency is preferably twice the frequency of the sampling clock of the desired base-band frequency subtracted from the transferred intermediate frequency. The selected clock frequency, however, is established so as to avoid Aliasing and the clock selected for the bandwidth of the base-band signal should be over the Nyquist rate.

05250000000000000000000000000000

“Aliasing” must be considered when the sampling signal is recovered. Aliasing occurs when the original signal cannot be distinguished or properly reconstructed due to an overlap of the recovered signal. When aliasing occurs, the original signal takes on the identity of a lower frequency, and information can be lost. That is, when the sampling frequency is lower than twice the signal bandwidth of the signal that is being repeatedly generated at the sampling period rate in a Fourier domain, the original signal begins to overlap itself. The original signal thus cannot be reconstructed even if a filter is used. Therefore, after the analog signal is converted to the digital signal, the digital signal can only be transformed back to the original signal using a sampling frequency over the Nyquist rate.

In order to convert the continuous analog input signal that has been passed through the above-described sampling process into the digital signal, a zero-order-hold circuit 302

is used, which distinguishes the amplitude of the signal, preferably at discrete time points.

The sampling signal, which is preferably in the form of a discrete time signal, is a continuous signal component repeatedly inputted at a prescribed frequency, generates the digital signal of the proper value according to the amplitude of the input signal.

5 At the same time, the under-sampling process occurs as the transferred clock frequency is inputted to the buffer 310. The under-sampling process is a process which applies the analog demodulation process to the digital demodulation process and intentionally aliases the signal. Generally, when the signal demodulated with the high frequency is converted by Analog-to-Digital conversion, it is sampled with the clock having a frequency of more than twice the corresponding frequency (the Nyquist Rate) to generate the digital signal. However, in the case of the under-sampling process, demodulation of the under frequency is accomplished at the same time as the Analog-to-Digital conversion takes place by using the Analog-to-Digital clock (which has a frequency of more than twice the bandwidth of the demodulated signal) with the frequency lower
10 than that of the modulated signal.
15

The under-sampling process occurs when the analog demodulation process is applied to the digital demodulation process. In general, when the signal modulated to the high frequency is converted from analog to digital, the clock having more than twice the subject frequency is used for the sampling to digitize the signal. In the case of the under-sampling, the clock with more than twice the frequency of the bandwidth of the signal
20

demodulated to the lower frequency than the modulated signal is used as the analog-to-digital clock, and the under demodulation of the frequency is performed at the same time as the analog-to-digital conversion takes place. The output frequency of the quantizer 303 is repeatedly performed throughout all band areas in the sampling frequency periods 5 during the sampling process. Therefore, among the output frequency of the quantizer 303, only the output frequency of the base-band quantizer is allowed to pass through the low-pass filter 210 to perform the demodulation process.

The clock inputted to the buffer 310 is supplied to the first and second output formatters 307 and 308 after the D flip-flop 311 performs a binary counting procedure. The output of the latch B 306, which is shifted one clock period from the output of latch A 305, is latched again to 0.5 times the frequency of the quantization output frequency. As a result, a QPSK demodulation signal shifted 90° out of phase with twice the periodic occurrences of the transmitted clock can be obtained.

The CDMA digital signal converted by the analog-to-digital converter is latched 15 by the latch 304 at more than twice the sampling periods transferred to the I channel and Q channel, before being transmitted to the latch A 305. The latch A 305 then transfers the I channel signal of the transferred base-band digital CDMA signal to a Finite Impulse Response (FIR) low-pass filter 210 at the desired base-band transferred periods via the first output formatter 307.

The Q channel is inputted to the latch B 306, and as the same latched signal having a delay of one sample period with a phase difference of 90° to the I channel having twice the sampling period is transferred to the second output formatter 307, the same function as the analog QPSK is accomplished.

5 That is, in the low-pass FIR filter 210, the unnecessarily repeated signal components generated during the "under-sampling process" and "Analog-to-Digital Conversion process" are removed before the base-band digital CDMA signal is transmitted to the switching station 212 through the PCM signal via the CDMA modem 211.

10 As described above, the base station demodulation apparatus of a CDMA mobile communication system in accordance with a preferred embodiment of the present invention has several advantages. For example, the digital signal of I channel and Q channel of the base-band can be directly demodulated in the intermediate frequency.

15 Additionally, since the Analog-to-Digital converter 209 is constructed to simultaneously perform the QPSK demodulation and Analog-to-Digital conversion, the number of circuit devices can be reduced and the circuit design can be simplified, resulting in a reduction of the power consumption, manufacturing costs, as well as overall size.

Moreover, since the digital FIR low-pass filter is used, phase linearity of the signal and noise reduction characteristics can be obtained.

Also, by using a Field Programmable Gate Array (FPGA), the alteration of the clock that is being used and the specific coefficients of the FIR low-pass filter can easily be reorganized, thereby the embodiment of the present invention can be applied to the various communication systems that use QPSK.

5 The foregoing embodiments and advantages are merely exemplary and are not to be construed as limiting the present invention. The present teaching can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art. In the claims, means-plus-function clauses are intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures.

0957
10 0957
0952 0950

WHAT IS CLAIMED IS:

1. A demodulation apparatus for a communication system, comprising:
 - an analog-to-digital converter device to convert an intermediate frequency signal into a digital signal and provide a quadrature component and an in-phase component of the digital signal;
- 5 a plurality of filters to filter components of the digital signal outputted from the analog-to-digital converter device in a low pass band respectively; and a CDMA modem to demodulate outputs of the plurality of filters.
2. The apparatus of claim 1, wherein said analog-to-digital converter comprises:
 - a digital sampler to sample the intermediate frequency signal;
 - a zero-order hold device to determine an amplitude of the sampled intermediate frequency signal;
- 5 a quantizer to convert the sampled intermediate frequency signal processed by the zero-order hold device to a digital signal;
- a plurality of latches to transmit the digital signal from the quantizer to a plurality of channels after a prescribed time delay; and
- 10 a plurality of output formatters to periodically output the latched digital signal transmitted to corresponding channels of the plurality of channels.

3. The apparatus of claim 2, wherein each of said plurality of output formatters comprises:

a plurality of negators to negate the latched digital signal and output a negated latched signal; and

5 a plurality of selectors one to one coupled to each of the plurality of
negators to select and output one of the negated latched signal and an unprocessed latched
digital signal.

4. The apparatus of claim 3, wherein the plurality of output formatters comprise first and second output formatters, and wherein the output of each output formatter is received by a low pass filter.

5. The apparatus of claim 1, wherein the plurality of channels comprise an In-phase channel and a Quadrature channel.

6. An analog-to-digital converter, comprising:
 - a digital sampler to sample an intermediate frequency signal;
 - a zero-order holder to determine an amplitude of the sampled intermediate frequency signal;

5 a quantizer to convert the sampled intermediate frequency signal processed
by the zero-order holder to a digital signal;

a plurality of latches to transmit the digital signal to a plurality of channels
after a prescribed time delay; and

a plurality of output formatters to periodically output the latched digital
10 signal transmitted to corresponding channels of the plurality of channels.

7. The apparatus of claim 6, wherein each of said plurality of output formatters
comprises:

 a plurality of negators to negate the latched digital signal and output a
negated latched signal; and

 a plurality of selectors to select and output one of the negated latched signal
and an unprocessed latched digital signal.

8. The apparatus of claim 7, wherein the plurality of output formatters
comprise a first and second output formatter, and wherein the output of each output
formatter is received by a low pass filter.

9. The apparatus of claim 6, wherein the plurality of channels comprise an I
channel and a Q channel.

10. A signal processor, comprising:

a digitizer, which receives an analog signal and generates a digital signal;

a channel separator, which receives the digital signal from the digitizer and separates the digital signal into at least 2 channels, each channel having a different phase;

5 and

a phase shift controller, which receives a clock signal and controls the phase shifting of the channel separator.

C-32351-D522610

11. The signal processor of claim 10, wherein the channels comprise a Q channel and an I channel having a phase difference of approximately 90°.

12. The signal processor of claim 10, wherein the analog signal is an intermediate frequency CDMA formatted signal.

13. The signal processor of claim 12, wherein an output of the signal processor is a QPSK modulated digital signal, having a first component and a second component out of phase with the first component.

5

14. The signal processor of claim 10, wherein the channel separator comprises:
a latch circuit, which receives the digital signal and outputs a first signal and
a second signal, wherein the second signal is a delayed first signal;
an output formatter, which receives the first and second signals and outputs
the first and second signals at prescribed periods.

15. The signal processor of claim 14, wherein the latch circuit comprises a first
latch, a second latch, and a third latch, wherein the output formatter comprises a first
output formatter and a second output formatter, and wherein the first latch receives the
digital signal from the digitizer, the second latch receives the output of the first latch and
provides the first signal to the first output formatter and the third latch, and the third
latch provides the second signal to the second output formatter.

16. The signal processor of claim 15, wherein the phase shift controller provides
the clock signal to the first, second, and third latches to control the phase shifting, and
provides a control signal to the first and second output formatters to control output
periods.

17. The signal processor of claim 15, wherein the first and second output formatters each comprise:

a plurality of negators, which receive and negate the corresponding first or second signal; and

5 a plurality of selectors to select and output one of the negated signal from the negator and the corresponding first or second signal, wherein each one of the plurality of negators is coupled to one of the plurality of selectors.

18. The signal processor of claim 10, wherein the digitizer comprises

a sampler, which receives and samples the analog signal;

a zero order hold circuit, which receives an output of the sampler and determines an amplitude of the received signal; and

5 a quantizer, which receives an output of the zero order hold circuit and generates the digital signal.

19. The signal processor of claim 10, wherein the phase shift controller comprises:

a plurality of buffers to receive and forward the clock signal; and

a logic circuit responsive to a buffered clock signal to generate a control

5 signal to control an output of the channel separator.

20. The signal processor of claim 10, further comprising a plurality of Finite Impulse Response (FIR) filters coupled to receive an output of the channel separator, wherein an individual FIR filter is coupled to each channel of the at least two channels.

21. A demodulator for a CDMA receiver, comprising:

an input circuit to amplify a filtered CDMA formatted input signal;

a first signal processor to generate an intermediate frequency CDMA signal

based on the amplified input signal;

a second signal processor to output first and second digital signals on first and second channels, respectively, based on the intermediated frequency CDMA signal, said second signal processor having an analog-to-digital converter to convert the intermediate frequency CDMA signal to an intermediate digital signal and a channel separator to generate the first and second digital signals based on the intermediate digital

10 signal; and

an output circuit to output a demodulated output signal based on the first and second digital signals, said output circuit having first and second Finite Impulse Response (FIR) filters to receive and filter the first and second digital signals, respectively, wherein the first and second digital signals have different phases.

ABSTRACT OF THE DISCLOSURE

A demodulation apparatus for a base station of a CDMA mobile communication system is provided, having an analog-to-digital converter device to convert an intermediate frequency signal into a digital signal and provide a quadrature component and an in-phase component of the digital signal, a plurality of filters to filter the components of the digital signal in the low pass band respectively, and a CDMA modem to demodulate the outputs of the plurality of filters. Since direct control by the digital signal of the base-band I channel and Q channel at the intermediate frequency can be performed and the analog-to-digital converter simultaneously performs the QPSK demodulation and the analog-to-digital conversion, the circuit design can be simplified and the characteristics reducing the noise can be obtained.

FIG. 1
(Related Art)

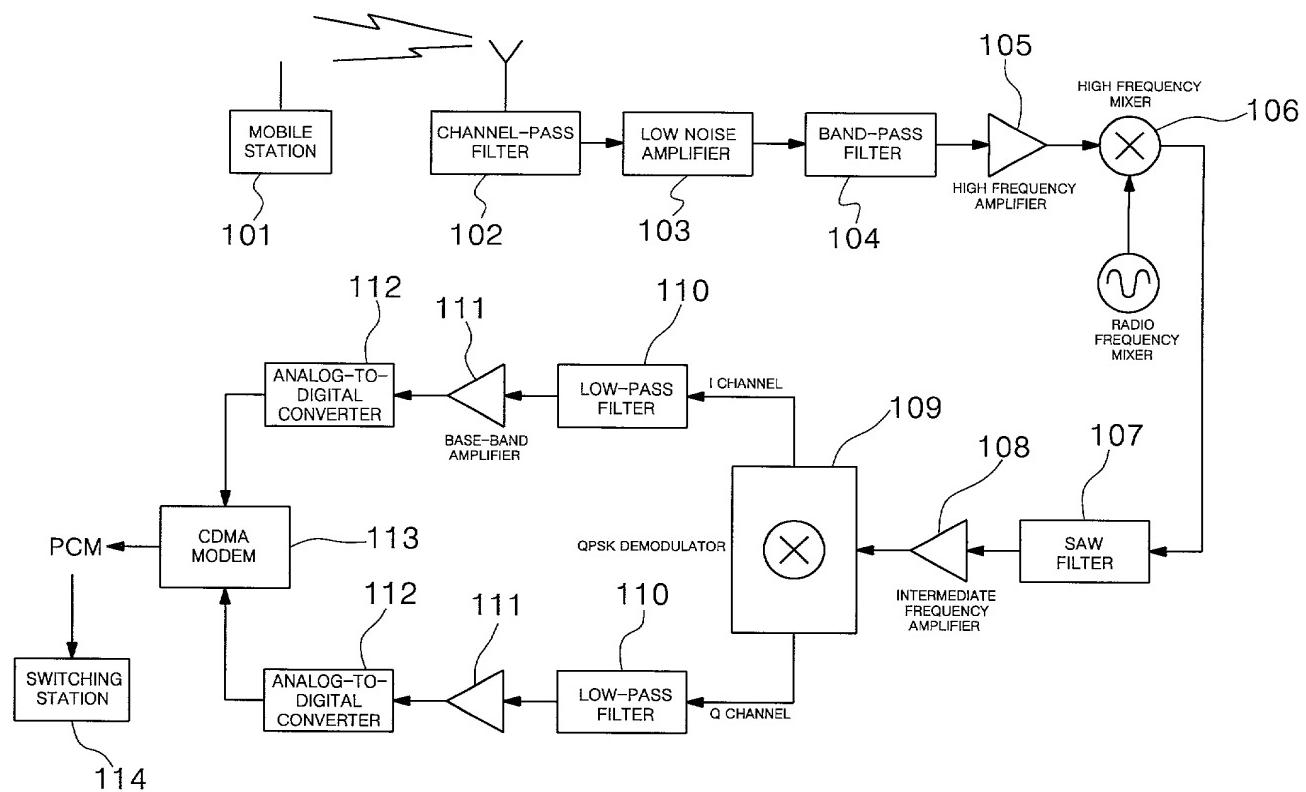


FIG. 2

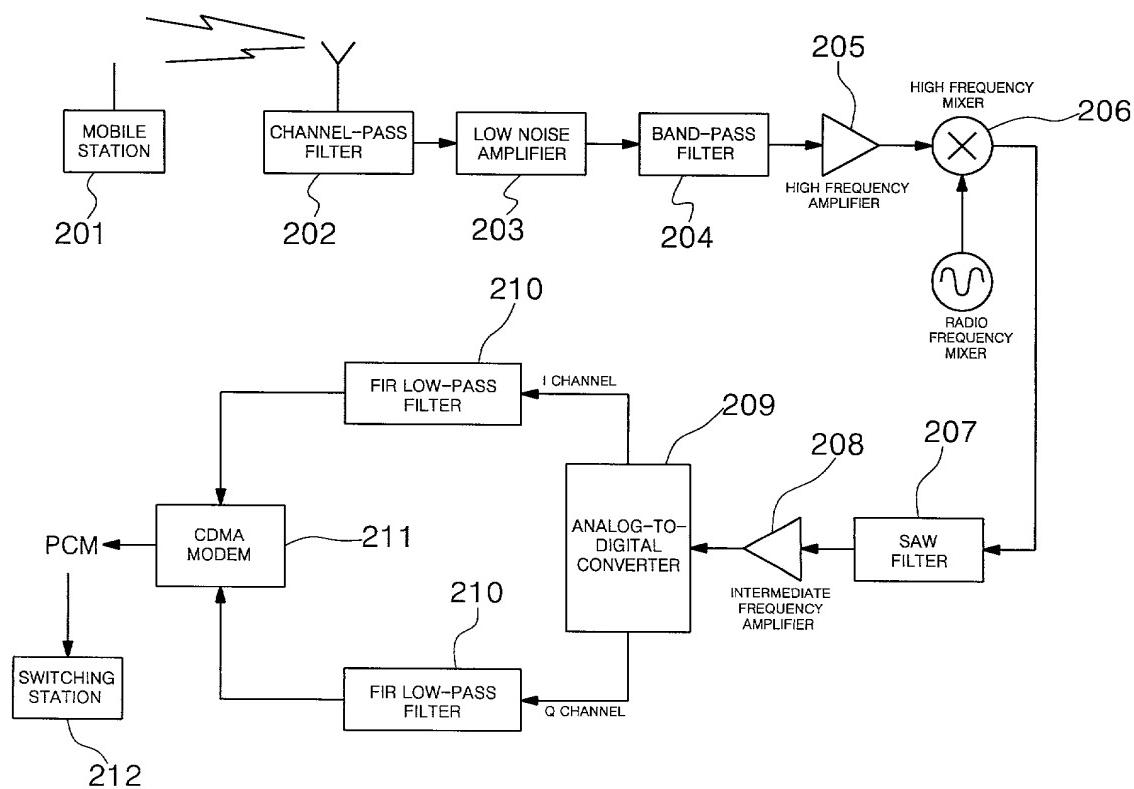


FIG. 3

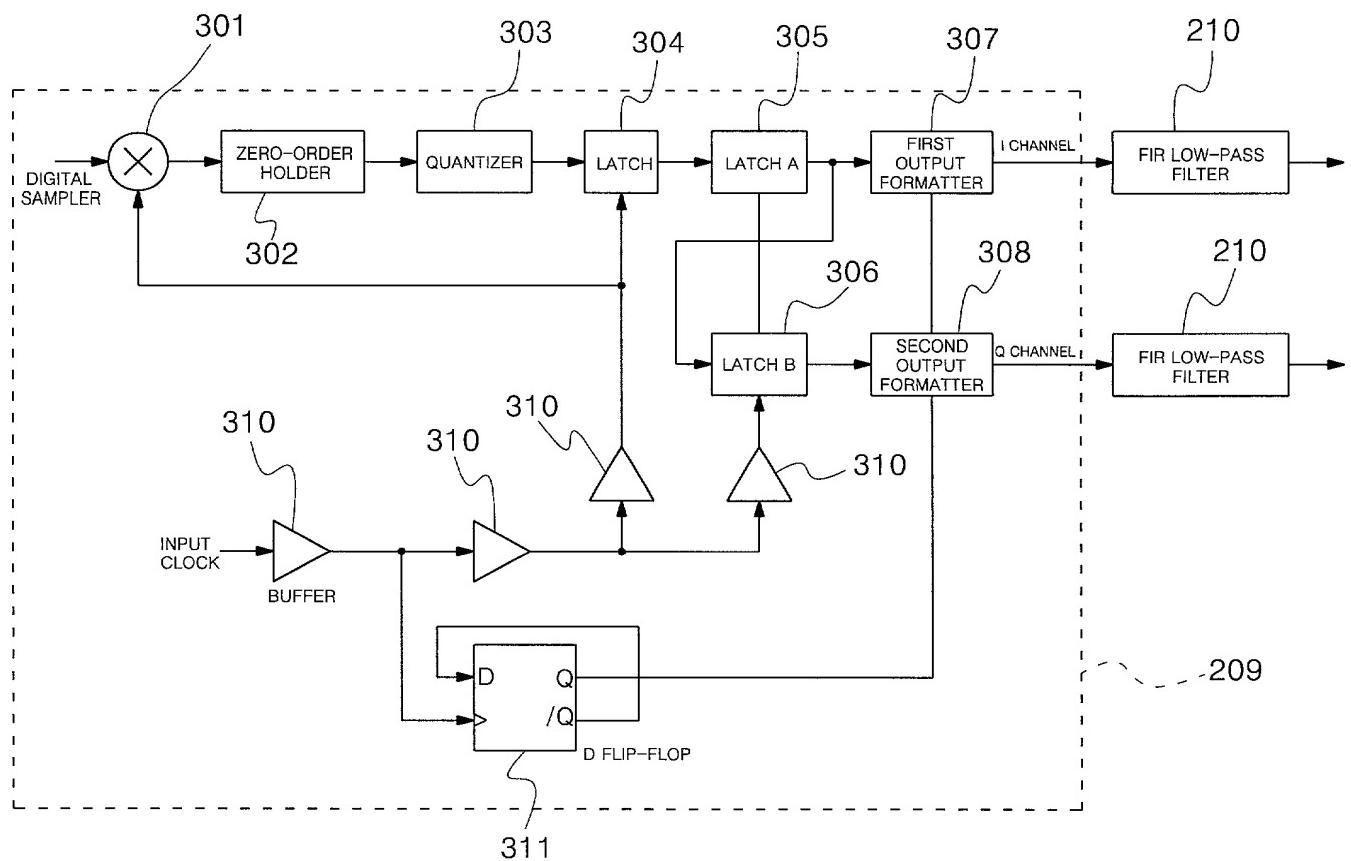
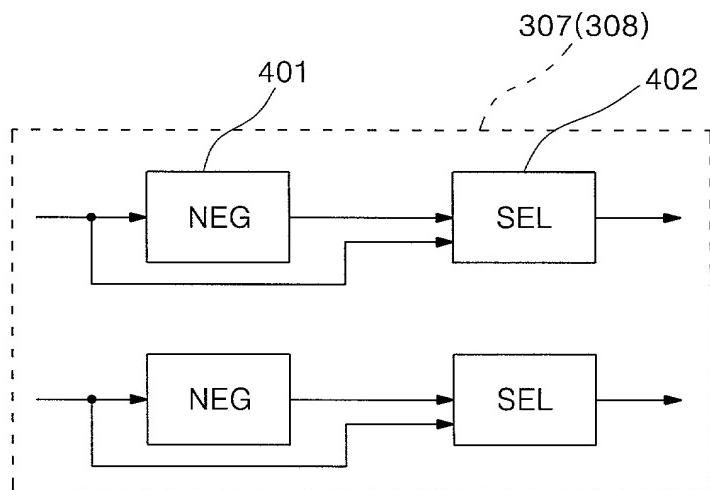


FIG. 4



DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter claimed and for which a patent is sought on the invention entitled A DEMODULATION APPARATUS OF A BASE STATION IN A CDMA MOBILE COMMUNICATION SYSTEM, the specification of which

[] is attached hereto [] was filed on _____ as Application Serial No. _____ and was amended on _____ (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by a amendment referred to above.

I acknowledge the duty to disclose information which is known to me to be material to patentability in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

<u>Prior Foreign Application(s):</u>	<u>Foreign Filing Date</u>
<u>Number</u>	<u>Month/Day/Year</u>
27090/1999	July 6, 1999

I hereby claim the benefit under 35 U.S.C.119(e) of any United States provisional application(s) listed below.

<u>Application Number(s):</u>	<u>Filing Date(Month/Day/Year)</u>

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

<u>Prior U.S. Application or PCT Parent Number</u>	<u>Filing Date(Month/Day/Year)</u>	<u>Parent Patent Number (if applicable)</u>

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statement may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint the following attorney(s) and/or agent(s): Daniel Y.J. Kim, Registration No. 36,186 and Mark L. Fleshner, Registration No 34,596; Carl R. Wesolowski, Registration No. 40,372, John C. Eisenhart, Registration No. 38,128, Rene A. Vasquez, Registration No. 38,6 Stuart I. Smith, Registration No. 42,159; Carol L. Druzbick, Registration No. 40,287; Anthony H. Nourse, Registration No. 46,121; and Ma A. Burke, Registration No. 34,474, all of

FLESHNER & KIM, LLP
P. O. Box 221200
Chantilly, Virginia 20153-1200

with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith, and all future correspondence should be addressed to them.

Full name of sole or first inventor: Won Hyoung PARK

Date:

Won Hyoung Park

2000. 5. 8

Residence: Kyunggi-do, Korea

Citizenship: Republic of Korea

Post Office Address: Kyungho Yunrip 303, 222, Yangji-dong, Sujung-gu, Sungnam-si, Kyunggi-do, Korea

Full name of joint inventor(s):

Inventor's signature:

Date:

Residence:

Citizenship:

Post Office Address:

Full name of joint inventor(s):

Inventor's signature:

Date:

Residence:

Citizenship:

Post Office Address:

Full name of joint inventor(s):

Inventor's signature:

Date:

Residence:

Citizenship:

Post Office Address:
